

Cortex®-A5, A7, A8, A9, A15, A17: Arm® Cortex-A Architecture Training - Face-to-Face Training

Objectives

You know the Cortex®-A architecture and can write software in C and Assembler. This is the perfect start for designing Arm based systems.

Participants

Software and hardware developers

Requirements

A basic understanding of ANSI-C and microcontrollers.

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Content

Cortex®-Ax Processor Architecture

- Operating modes, states, pipeline, register organization
- User mode, fast interrupt (FIQ) mode, interrupt (IRQ) mode
- Supervisor mode, system mode, undefined mode, secure monitor mode
- Thumb-2 state, Arm state, Jazelle state, ThumbEE state
- Cortex®-Ax register file
- Status register

Arm Processor Cores: Overview

- Cortex®-M, Cortex®-R, Cortex®-A processor cores
- Arm7 / Arm9 / Arm10 / Arm11

Arm, Thumb-2 and DSP Instruction Sets

- v7 Thumb-2 instruction set
- Arm/Thumb interworking
- Most important assembler directives
- v4, v4T, v5, v6 instruction set overview

Advanced SIMD and VFP Extension

- NEON coprocessor
- VFP floating point unit

Jazelle RCT Extension Overview

- Thumb-2EE instruction set
- ThumbEE state

Exception Handling

- Exception modes: FIQ, IRQ, ABORT, UNDEF, SVC, SMC
- Exception handler templates
- Vector tables: normal, secure, monitor mode
- TrustZone (secure) exception handling
- Exception handling in singlecore and multicore systems
- Global interrupt controller (GIC)
- Vector interrupt controller (VIC)

System Control Coprocessor, CP15

- Arm coprocessor concept, CP0 ... CP15

- Overall system control & configuration
- Cache configuration and cache management
- Memory management unit (MMU) configuration
- System performance monitoring (PMU)

Level 1 Memory System

- Instruction and data cache
- Cache initialization
- Store buffer

Level 2 Memory System

- Advanced microprocessor bus architecture (AXI)
- AXI bus masters
- AXI bus slaves
- Second level caches
- Preload engine (PLE)
- On-chip RAM and flash, peripherals
- External memory interface (EMI)

Memory Management Unit MMU

- Translation lookaside buffer (TLB)
- Translation and page tables, attributes
- Virtual addressing, tablewalk

Cortex®-Ax Multiprocessor Core

- Primary, secondary CPU
- Global interrupt controller (GIC)
- Snoop control unit (SCU)
- Accelerator coherency port (ACP)
- Address filtering

Startup Singlecore System

- Startup file
- Vector table, stack, PLL and data initialization
- Cache, MMU and branch predictor initialization
- From reset to main

Startup Multicore System

- From reset to main
- Primary CPU initialization
- Secondary CPU initialization

Clock, Reset and Power Control

- Low power modes

TrustZone Extension

- TrustZone overview
- Secure monitor mode
- TrustZone exception handling
- Startup in Secure world
- Switch from Secure world to Non-secure world

Virtualization Extension

- Hyp mode
- Hypervisor
- Large address extension
- L1 and L2 tablewalk

Cortex®-Ax Debug Support

- Embedded trace macrocell (ETM)
- Program trace macrocell (PTM)
- CoreSight debug components
- Performance monitoring unit (PMU)
- Cross trigger unit
- Debug coprocessor, CP14

Software Development Overview

- CMSIS for Cortex®-A
- Compiler options
- Linker options
- Description file
- Locating program and data in memory

Practical exercises on all topics with IAR Workbench and an evaluation board

FACE-TO-FACE TRAINING

Price * Duration

- 4 days

Training code: E-CORAX

* Price per attendee, in Euro plus VAT

Face-To-Face - German

Duration

4 days

Live Online - German

Duration

4 days

Coaching

Our coaching services offer a major advantage: our specialists introduce their expertise and experience directly in your solution process, thus contributing to the success of your projects.

We will be happy to provide you with further information or submit a quotation tailored to your requirements.